# 

# United States International University

Spring Semester 2014

##### MIS6010 : IT Infrastructure

##### (Course Outline)

***LECTURER: DR. G. CHEGE*;**

**email:** [***gchege@usiu.ac.ke***](mailto:gchege@usiu.ac.ke)**; Location*:* ICT Building– 3rd Flr. Rm. 4**

**Class Times: Friday 5.40 - 9.00 pm (Lab 3)**

**Office Hours: Tuesday/Thursday 10.00am - 11.00am; 1.00pm - 3.00pm;**

**COURSE DESCRIPTION**

The purpose of this course is to conduct a study of the evolution of computer architecture and the factors influencing the design of hardware and software elements of computer systems. Topics include: instruction set design; processor micro-architecture and pipelining; cache and virtual memory organizations; protection and sharing; I/O and interrupts; in-order and out-of-order superscalar architectures; VLIW machines; vector supercomputers; multithreaded architectures; symmetric multiprocessors; memory models and synchronization; embedded systems; and parallel computers.

*Pre-requisites: none*

*Credit Units: 3*

**Link to University Mission Outcomes and School of Science & Technology**

**(a.) University Mission outcomes**

The course content for IST6000 directly contributes to the attainment of University Mission Outcomes in:

* Higher Order Thinking (U1)
* Literacy (U2)
* Preparedness for Career (U3)

**Teaching and Learning Methods**

Lectures will introduce the main principles in the key areas of Computer Architecture, communication systems, and programming. Tutorial sessions will be used for a deeper and wider discussion of material covered in lectures. Practical sessions will be used for hands-on experience of low-level language programming.

**Course Learning Outcomes**

At the end of this course students should be able to:

1. Explain how computers are organized.
2. Identify and explain what influences have determined the architectures of processors, memory systems, and input/output systems.
3. Evaluate and improve computer system performance through analysis and computer simulation.
4. Explain the fundamentals of pipelining, caches, and virtual memory.
5. Write assembly language programs.

**COURSE OUTLINE**

|  |  |  |  |
| --- | --- | --- | --- |
| **WEEK** | **LECTURE/TOPICS** | **READINGS** | **ASSIGNMENTS/ LABS** |
| Week1 | **1) Introduction**  Languages, Levels, and Virtual Machines; Contemporary Multilevel Machines ; Evolution of Multilevel Machines; Milestones In Computer Architecture:  The Zeroth Generation–Mechanical Computers; The First Generation–Vacuum Tubes  The Second Generation–Transistors; The Third Generation–Integrated Circuits  The Fourth Generation–Very Large Scale Integration; The Fifth Generation–Low-Power and Invisible Computers; The Computer Zoo; Technological and Economic Forces; The Computer Spectrum; Disposable Computers; Microcontrollers; Mobile and Game Computers  Personal Computers; Servers; Mainframes; Example Computer Families; Introduction to the x86 Architecture; Introduction to the ARM Architecture; Introduction to the AVR Architecture; Metric Units | Chapter 1 (Tannenbaum) |  |
| Week 2 | **2) Structured Computer Organization** CPU Organization; Instruction Execution; RISC versus CISC; Design Principles for Modern Computers; Instruction-Level Parallelism; Processor-Level Parallelism; Primary Memory; Bits; Memory Addresses; Byte Ordering; Error-Correcting Codes; Cache Memory; Memory Packaging and Types; Secondary Memory; Memory Hierarchies; Magnetic Disks; IDE Disks; SCSI Disks; RAID; Solid-State Disks; CD-ROMs; CD-R/CD-W; DVD; Blu-ray; INPUT/OUTPUT;  Buses; Terminals; Mice; Game Controllers; Printers; Telecommunications Equipment; Digital Cameras; Character Codes | Chapter 2 (Tannenbaum) |  |
| Week 3 | **3) Digital Logic Level** Gates; Boolean Algebra; Implementation of Boolean Functions; Circuit Equivalence ; BASIC DIGITAL LOGIC CIRCUITS: Integrated Circuits; Combinational Circuits; Arithmetic Circuits ; Clocks; MEMORY: Latches Flip-Flops; Registers; Memory Organization; Memory Chips; RAMs and ROMs; CPU CHIPS AND BUSES 185 CPU Chips; Computer Buses; Bus Width; Bus Clocking; Bus Arbitration; Bus Operations; EXAMPLE CPU CHIPS: The Intel Core i7; The Texas Instruments OMAP4430 System-on-a Chip; The Atmel ATmega168 Microcontroller; EXAMPLE BUSES: The PCI Bus; PCI Express; The Universal Serial Bus; INTERFACING  I/O Interfaces; Address Decoding | Chapter 3 (Tannenbaum) | Assignment1 |
| Week 4 | 4a) Instructions: Language of the Computer  Introduction  Operations of the Computer Hardware  Operands of the Computer Hardware  Signed and Unsigned Numbers  Representing Instructions in the Computer  Logical Operations  Instructions for Making Decisions  Supporting Procedures in Computer Hardware  Communicating with People | Chapter 2 (Patterson/Hennessy) | Lab #1 |
| Week 5 | 4b**) Instructions: Language of the Computer**  MIPS Addressing for 32-Bit Immediates and Addresses  Parallelism and Instructions: Synchronization  Translating and Starting a Program  A C Sort Example to Put It All Together  Arrays versus Pointers  Advanced Material: Compiling C and Interpreting Java  Real world example: ARM Instructions  Real world example: x86 Instructions  Historical Perspective | Chapter 2 (Patterson/Hennessy) | Assignment#2  Lab #2 |
| Week 6 | **5a)The Processor**  Introduction  Logic Design Conventions  Building a Datapath  A Simple Implementation Scheme  An Overview of Pipelining | Chapter 4 (Patterson/Hennessy) | Term Paper |
| Week 7 | **5b)The Processor**  Pipelined Datapath and Control  Data Hazards: Forwarding versus  Parallelism and Advanced  Real Stuff: the AMD  Advanced Topic: an Hardware Design and More Pipelining | Chapter 4 (Patterson/Hennessy) | Mid Term Exam |
| Week 8 | 6a) Large and Fast: Exploiting Memory Hierarchy  Introduction  The Basics of Caches  Measuring and Improving Cache  Performance  Virtual Memory  A Common Framework for Memory | Chapter 5 (Patterson/Hennessy) | Lab #3 |
| Week 9 | **6b) Large and Fast: Exploiting Memory Hierarchy**  Hierarchies; Virtual Machines  Using a Finite-State Machine to Control a Simple Cache  Parallelism and Memory Hierarchies: Cache Coherence  Advanced Material: Implementing Cache Controllers  Real Stuff: the AMD Opteron X4 (Barcelona) and Intel Nehalem  Memory Hierarchies | Chapter 5 (Patterson/Hennessy) | Assignment#3 |
| Week 10 | **7a) Storage and Other I/O Topics**  Introduction  Dependability, Reliability, and Availability; Disk Storage  Flash Storage  Connecting Processors, Memory, and I/O Devices | Chapter 6 (Patterson/Hennessy) | Lab #4 |
| Week 11 | **7a) Storage and Other I/O Topics**  Interfacing I/O Devices to the Processor, Memory, and Operating System  I/O Performance Measures: Examples from Disk and File Systems  Designing an I/O System  Parallelism and I/O: Redundant Arrays of Inexpensive Disks  Real world example: Sun Fire x4150 Server  Advanced Topics: Networks  Historical Perspective | Chapter 6 (Patterson/Hennessy) |  |
| Week 12 | **8a) Multicores, Multiprocessors, and Clusters**  Introduction  The Difficulty of Creating Parallel Processing  Programs  Shared Memory Multiprocessors  Clusters and Other Message-Passing  Multiprocessors  Hardware Multithreading  SISD, MIMD, SIMD, SPMD, and Vector | Chapter 7 (Patterson/Hennessy) | Presentations |
| Week 13 | **8b) Multicores, Multiprocessors, and Clusters**  Introduction to Graphics Processing Units  Introduction to Multiprocessor Network Topologies  Multiprocessor Benchmarks  Roofline: A Simple Performance Model  Real world example: Benchmarking Four Multicores Using the Roofline Model; Historical Perspective | Chapter 7 (Patterson/Hennessy) |  |
| Week 14 | Final Exam |  |  |

**Mode of Delivery**

The lecture and question and answer methods will be used to introduce the main principles in the key areas of computer architecture, communication systems, and programming. Tutorial sessions will also be held for a deeper and wider discussion of content and material covered during lectures. Students are expected to participate actively in class and attend all sessions on time.

Regular attendance and active participation in this class are expected. This is a course that is experiential and requires active involvement to gain maximum benefit. To get involved you must attend class, spend time on the textbooks, WWW and all other provided materials in independent study.

**Instructional Materials and/or Equipment**

Course text, Journals, Presentation slides, Handouts, Smart/White board, Blackboard e-learning platform, Microprocessor kits, Assembly language, Internet/WWW.

**TEXTBOOKS**

**Core Reading Materials**

1. Patterson, D. A., Hennessy, J.L. (2011). *Computer Organization and Design: The Hardware/Software Interface.* 5th Edition, San Mateo, CA: Morgan Kaufman.
2. Andrew S. Tannenbaum (2013) *Structured Computer Organization*, 6th Ed. Prentice-Hall.

**Recommended Reference Materials**

1. Hennessy, J. L., Patterson, D.A. (2007). *Computer Architecture: A Quantitative Approach.* 3rd Edition, San Mateo, CA: Morgan Kaufman.
2. [Williams, R. (2006). *Computer Systems Architecture: a Networking Approach*. 2nd E](http://books.google.com/url?id=y1BuoXpPX3kC&q=http://www.pearsonhighered.com/educator/academic/product/1,3110,0321340795,00.html&linkid=2&usg=AFQjCNENcETxHvt86wiYeovrrgU5E2sqlw&source=gbs_web_references_r&cad=5)dition, Upper Saddle River, New Jersey: Prentice Hall.

**COURSE EVALUATION**

***Grading***   
Your final grade will be based on several indicators of performance.

**MARK DISTRIBUTION**

|  |  |
| --- | --- |
| **BASIS OF EVALUATION** | **PERCENTAGE** |
| Assignments | 15 % |
| Group Term Project/Case Analysis | 20 % |
| Lab Assignments | 15 % |
| Midterm Exam | 20 % |
| Final Exam | 30 % |

**Case Study Presentation**: The textbook introduces at the end of each chapter a case study. You will study these cases and be ready to defend issues to the class at the beginning of the next lecture.

**Term Paper/ Project/ Case Analysis**: each group will be assigned a case for analysis and presented to the class in the last two weeks of the semester.

**Exams**: The exams will cover all chapters listed on the schedule, the material discussed in class lectures, all additional handouts, the term project and the assignments during the Semester until the time point of examination.

***Assignments***

The assignments are designed to be active learning experiences, supplementing class discussions and reading assignments.

**NOTES**

Notes will be made available online, in Blackboard.

**READINGS**

You are expected to read all materials that are mentioned in the above table in the column "Readings" for the assigned week in advance so that you are well prepared for lectures and tutorials. Otherwise you won't be able to participate actively in the lectures and can't complete the tutorials.

**GRADING SYSTEM**

90 – 100 = A 87 – 89 = A- 84 – 86 = B+

80 – 83 = B 77 – 79 = B- 74 – 76 = C+

70 – 73 = C 67 – 69 = C- 64 – 66 = D+

62 – 63 = D 60 – 61 = D- 0 – 59 = F